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A Review on Challenges and Advances in On-Chip Antenna Design for Millimeter Wave Applications

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Abstract

High speed, large bandwidth for short distance wireless communication has made unlicensed millimeter-wave (mm-wave) band best suitable for the design of 60 GHz WPAN systems. Moreover the demand for high level of integration and miniaturization involves design of antenna along-with the front end circuits on the same chip leads to System On-Chip design. This paper presents a comparative discussion on various On-Chip antenna designs proposed in different CMOS technologies. Discussion starts with a brief introduction of applications and regulations of 60GHz wireless communication followed with the gain and efficiency limitation of Antenna On-Chip (AoC) solution designed over Silicon substrate

Key Words: 60GHz, On-Chip Antenna, Silicon, CMOS Technology

Introduction

New wireless applications in low frequency band which is already overcrowded demanded for high frequency band. Therefore signals in the frequency range from 100 GHz to 3 THz have led to the recent increase in research efforts. IEEE 802.15.3 [1] group has investigated 7 GHz band spectrum around 60 GHz as an alternate, therefore opening of 60GHz license [2] free spectrum for millimeter waves applications such as ground based radio astronomy, radiometry operation and broadband radio communication requires fast data transfer. Wireless Personal Area Network (WPAN) requires a large to support high speed and point-to-point communication [3]. A worldwide allocation of 60GHz with almost same bandwidth was released. In 2000 Japan [4] first released 7GHz band in 60GHz spectrum. The Federal Communications Commission (FCC) in United States [5], has aimed for 7 GHz bandwidth (57-64 GHz) around 60 GHz for unlicensed use. At the same time other governments have allowed 60 GHz band to be used without any license. The allocation of the frequency kept different in each country and all the bands commonly share a continuous bandwidth of 7 GHz centred at 60 GHz. Few years later Canada [6], Australia, North America and Europe [7-9] also issued the band. A maximum power limits to 10 dbm and maximum allowed antenna gain of 47dbi was proposed to regulate the link budget. Table.1 shows the worldwide allocation of 60GHz band.

Table 1: Gain and Transmission power allocation for 60 GHz band

Countries	Frequency Band (GHz)	Maximum Tx power (mW)	Maximum Antenna Gain (dBi)
Japan	59-66	10	47
USA	57-64	500	-
Canada	57-64	500	-
Australia	59.4-62.9	10	-
Europe	57-66	20	37
China	59-64	10	34
Korea	57-64	10	-

In [10] propagation measurement realized the justification of 60 GHz radio technology for non-licensing applications.

Conventional integration of Antenna module, RF module over high frequency is a little bit challenge for design engineer. A large amount of area is consumed whether horizontal or vertical integration [11] of modules is done, as being the largest component of the design antenna remains outside of the chip. GaAs based transceiver are

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best suitable for 60GHz radios [12-14] but suffers with the problem of low cost and minimal integration. Therefore Silicon based semiconductor technology such as CMOS and SiGe, which is most suitable for Integrated circuits, proposes on-chip integration of RF front ends and antenna as shown in Fig1.

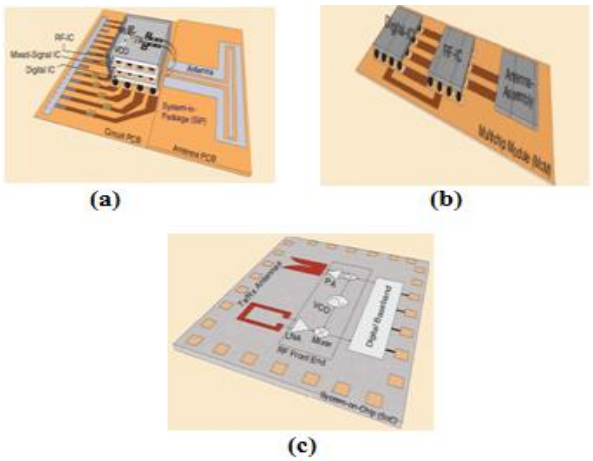

Fig.1. Antenna integration in various transceiver modules (a) System-in-package(SiP) [11] (b) Multichip module(MCM) [11] (c) System-on- chip(SoC) [11]

Integration of digital circuitry followed from the prediction of Moore which becomes double for every 18 months; lead the excessive down scaling of transistor size. Therefore various semiconductor nodes were proposed as enlisted in the table 2.

Table2: Semiconductor node technology development over years

Year	1997	1999	2001	2004	2006
Process node	250 nm	180 nm	130 nm	90 nm	65 nm
Year	2008	2012	2014	2017	2018
Process node	45 nm	22 nm	14 nm	10 nm	7 nm

In past years [26-27] many developments has taken place in on-chip antenna design. This paper presents survey in advances, challenges and state of art in the field of on-chip antenna design. Section II discusses restrictions on the design shapes and DRC, section III presents state of art and silicon substrate challenges, in section IV equivalent model and radiation efficiency is discussed. Section V presents the various techniques used so far to enhance the gain, section VI and VII contains application and conclusion respectively.

On-Chip Antenna Layout And Design Rule Check

In a single chip RF transceiver usually antenna is integrated with LNA or PA using T/R switch [29] as shown in Fig 2, due to antenna characterization problem, in most of the transceiver designs on-chip antenna gain is not mentioned separately.

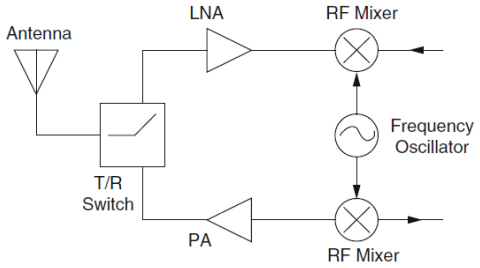

Fig.2. Transceiver on a single chip.

Initially an On-Chip antenna implemented in 0.18-µm technology was successfully demonstrated [15] for intra-chip wireless interconnect at comparatively low frequency of 15GHz. Four types of antenna monopole [16], dipole [17], yagi and loop antenna are most popular for on-chip design as shown in the Figure3. At 60GHz [18] an Inverted-F and quasi yagi antenna designed.

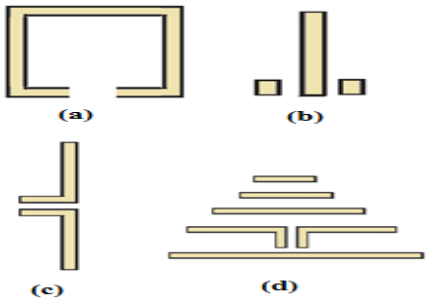

Fig.3. Different on-chip antenna structures (a) Loop antenna (b) Monopole antenna (c) Dipole antenna (d) Yagi antenna

Most of loop, dipole, multi-turn dipole, slot tapered are presented [17][19-25] but suffers from negative gain. Various structures such as elliptical, ring, patches and circle cannot be used because of the strict design rules in standard CMOS process, which limits the maximum allowed width and spacing. Silicon substrate has low resistivity ρ=10 Ω-cm and ε_r=11.9, standard thickness is 300~500µm depending upon the various nodes. Multiple metal layers M_1-M_7 are stacked over the substrate inside the SiO_2 layer, which has typically a total thickness of 10~15µm. M_1-M_7 has a thickness of 0.2~1.2 µm, more than 15µm separation is not allowed between the top and bottom metal layers as shown in Figure.4.

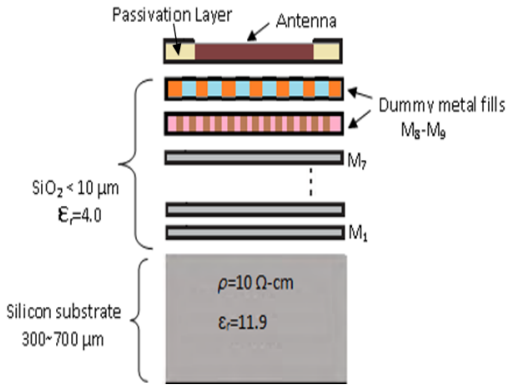

Fig.4. Multiple metal layers structure in standard CMOS process.

Transistors constructed over silicon substrate in the top region where doping is done and on-chip antenna in the top layer. SiO_2 layer acts as insulator between the metal layers, can be connected through the metal vias. M_1-M_7 serves two purposes; first they can be used in the design of passive components of inductors and capacitors and second they can also be used for metal interconnects. Silicon Nitride is used as a passivation layer. Metal widths have to be designed according to the highly restrictive foundry rules. In order to maintain Copper current density rules and maximum allowed metal widths, dummy metal fillings is necessary for all metal layers, M_8 and M_9 are used for this purpose. To satisfy the design rule check (DRC) change in radiation pattern and efficiency can be easily observed, which in turn also limits the geometry of antenna. Ground is provided at the bottom of the substrate for off chip and some of the designers also used M_1 for this purpose. Various standard CMOS process node does not allow metal widths more than a certain limit, in 0.18µm design M_1 can take maximum 30µm width, 500 µm length with minimum spacing of 3~4 µm and slant strip can be designed 45^0 maximum as shown in Figure 5. Similarly in 65 nm the maximum allowed length width and spacing are 300 µm, 25 µm and 1.5 µm respectively. In 28nm these maximum widths, lengths and spacing are 20 µm, 250 µm and 1 µm respectively. BEOL process also used for on-chip antenna design and its design rules are more challenging as of strict limitations. Therefore the solid patches of any shape cannot be implemented in CMOS process.

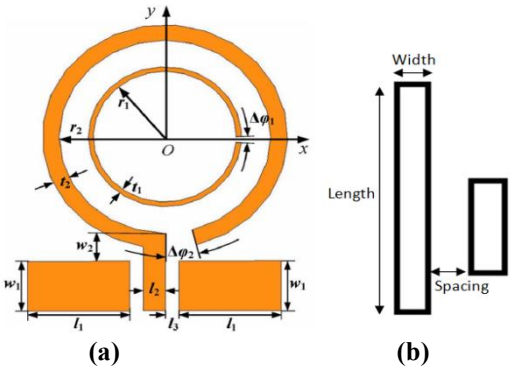

Fig.5. (a) On-Chip antenna [44] (b) Basic DRC checks

Therefore an antenna designer must also have the knowledge of IC design.

On-Chip Antenna Substrate Limitation And State Of Art

Apart from the discussed layout challenges on chip antenna design has some major benefits. Conventionally antennas are designed on PCB therefore maximum power transfer is always required when two components or networks are interfaced with each other; this is accomplished only if perfect matching is done. Conventionally 50Ω matching boundary always exists between RF front end circuits and antenna. Co-design of antenna with LNA (in case of receiver) and PA (in case of receiver) ensures that impedances of both are complex conjugate to each other hence eliminates this limitation. Loss in AoC is also minimal because of the removal of bonding wire interconnects. On chip antenna suffers from the problem of low efficiency and gain, major contributor to this problem are low resistivity and high dielectric constant of substrate material. Silicon substrate has low resistivity ρ= 10 Ω-cm which makes it favourable for IC design, low resistivity avoids latch-up [28] problem but for antenna RF power instead of radiating leaks through the low resistivity substrate and causes loss in the form of heat. Similarly high dielectric constant causes most of power trapped inside substrate. Both of the reasons causes drastic drop in the radiation efficiency, only 3% efficiency for a dipole antenna [29] and 11.5% in other design [30] at 60GHz. So far challenges and benefits of on-chip antenna have been discussed, a comparative analysis and state-of-art of some on chip antenna has been reported in the table3.

Table 3: Summary and comparison of state of art on-chip antenna

Only a very few stand alone designs have been proposed, most of the design includes complete performance measurement of transceivers. Majority of listed antennas are reported in 0.18µm , 0.13µm and 90 nm, only a few designs have been reported in 65 nm, 45 nm. Individual antenna gain measured is also not shown in some designs because of poor radiation efficiency and negative gain. Differential architecture helps in improving signal to noise ratio (SNR) and ease in integration therefore accepted by majority of the designers. Some of them designs are also proposed in SiGe process.

On-Chip Antenna Modelling & Efficiency

Design optimization is possible if the equivalent circuit parameters of the on-chip antenna are known, especially when impedance matching impact in co-design is to be evaluated. Commonly used Dipole and its equivalent model [31] is shown in the Figure 6. Silicon substrate is represented with R_{sub} and C_{sub} in shunt, R_{sub} is due to the conductivity of the substrate and C_{sub} exists when because dielectric material is sandwiched in between M_1 and off chip ground.

Silicon dioxide layer also causes C_{ox} capacitance connected in series with the shunt substrate components. Surface wave losses, radiation losses and conductor losses of the dipole are represented with R_{sur}, R_r and R_c respectively. If on-chip ground is used instead of off-chip ground then C_{ox} can be shorted.

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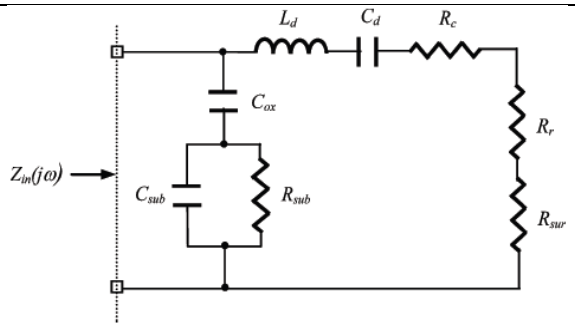

Fig.6. On-chip dipole antenna equivalent model with off-chip shield.

All these are modeled in series along with substrate equivalents. C_d and L_d are diploe capacitances and inductances respectively. Low resistivity silicon substrate causes small radiation resistance R_r, which ultimately results in poor radiation efficiency.

$$R_r \, \alpha \int_{\theta} \int_{\emptyset} \frac{k_o w_d \varepsilon_{eff}}{h} d\theta d\emptyset \qquad (1)$$

Where h is substrate thickness, w_d dipole width and k_0 is wave vector. ε_{eff} is effective dielectric constant[30]

$$\varepsilon_{eff} = \frac{\varepsilon_{eq}+1}{2} + \frac{\varepsilon_{eq}-1}{2\sqrt{1+10h/w_d}} \qquad (2)$$

where ε_{eq} is equivalent permittivity of multiple layers. Conductor loss is given by

$$R_c = \frac{l_d}{w_{eff}} \sqrt{\frac{\mu_o R_{sh} t_d f}{\pi e^{-t/\delta}}} \qquad (3)$$

where l_d is dipole length, R_{sh} is heet resistance, t_d is metal thickness, δ is skin depth and w_{eff} is effective width. Surface wave resistance is given as

$$R_{sur} = \frac{Z_0^2}{2P_{sur}} \qquad (4)$$

Z_0 is the characteristic impedance and P_{sur} is the surface wave power of TM_0 surface wave propagation mode [32]. All these losses results in the coupling of noisy currents from the antenna to the nearby active devices such as transistor through silicon substrate. These electrical disturbances results in crosstalk, which is to be optimised in the co-design of layout, otherwise it will cause shift in the radiation pattern of on-chip antenna. Once the loss mechanisms are identified it is also possible to minimize them, few of them are discussed here.

A. Substrate Thinning

Surface wave modes can be eliminated by thinning the silicon substrate to less than a $\lambda_g/4$, thinning does not remove TM_0 mode. Constructive interference between the direct radiated field reflected from ground and refracted field from the interface joining substrate and air improves the radiation efficiency. Strength of TM_0 surface wave is very weak and it undergoes a large attenuation during propagation, for silicon substrate if the substrate thickness is chosen five times lesser then this mode can be used to enhance gain. Efficiency of on-chip antenna [33] got doubled around 23% at 60GHz after substrate thinning to 241µm.

B. Proton Implantation

For a high gain antenna high resistivity substrate is best suited, this is contradictory to the fact that silicon substrate has low resistivity, substrate resistivity can be improved from 10Ω-cm to 10^6Ω-cm with selective proton implantation [16] so that it does not trigger latch-up.

C. Micromachining

Selective removal of bulk silicon in a small region at the back side of substrate is done by dry or wet etching. Crystal planes in the substrate limits the wet etching leaves slanted walls, but with a promise of batch execution process so that large number of wafers can be handles just by submerging them into the solution. Radiation efficiency improved to 77% [34] and 93.9% [35] has been presented.

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D. Superstrate Focusing

A superstate layer of high permittivity in chosen at the top of the slot layer, these superstates act as antenna part and hence improves the antenna directivity and radiation efficiency[36]. It has been shown that more than 30% radiation efficiency [37] has been observed.

E. Silicon Lens

It is post processing step where silicon lens is used at the back of convex shaped bulk substrate to convert surface wave power in to useful radiated power, hence improved [38-39] gain has been observed with this method.

F. Quartz and Dielectric Resonator

Image currents suppressed to improve radiation efficiency with the help of dielectric resonator antenna [40-41] and quartz loaded antenna [42] has shown improved efficiency more than 30%.

G. Artificial Magnetic Conductor

Artificial magnetic conductors (AMC) are high impedance surfaces posses reflection coefficient Γ=+1, therefore these surfaces are inserted in the different metal layers beneath antenna, inside oxide layer to produce image currents such that these image currents constructively interfere with the reflected wave from the off chip ground. AMC as a reflector has been successfully demonstrated and widely adopted as most popular solution in many of on-chip antenna designs [43-50]. These AMC surfaces are planar therefore can be easily incorporated in the design reducing the requirement of connecting vias with 5-10 % improvement in efficiency.

On-Chip Antenna Application

On-chip antenna has promised variety of applications such as MEMS antenna co-design, wireless intra chip communication for clock distribution, highly integrated imagers and radars.

Conclusion

This paper presents the comparative design aspects in various CMOS process nodes and integration of antenna with RF front end circuits to meet technology demand for high speed data transfer. Co-design of components, integration and modelling to understand crosstalk due to low resistive silicon substrate. Strict layout design rules and limitations in system-on-chip(SoC) design, different economic and commercial approaches adopted to enhance antenna efficiency, still a lot of efforts to be done to overcome these limitations in more efficient way in near future.

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